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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,770	08/07/2001	Avner Pierre Badehi	42043	2264
1609	7590	12/01/2004	EXAMINER	
ROYLANCE, ABRAMS, BERDO & GOODMAN, L.L.P.			BEREZNY, NEMA O	
1300 19TH STREET, N.W.				
SUITE 600				
WASHINGTON,, DC 20036				
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/922,770

Applicant(s)

BADEHI, AVNER PIERRE

Examiner

Nema O Berezny

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20,22-24,26-29,33,34,36 and 38-67 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20,22-24,26-29,33,34,36 and 38-67 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/725,166.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10-19-04 has been entered. Claims 20, 22-24, 26-29, 33-34, 36, 38-67 is currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 20, 22-23, 26-28, 34, 38-45, 48, 52-55, 59-61, and 63-64 are rejected under 35 U.S.C. 102(a) as being anticipated by Salatino et al. (5,915,168). Salatino discloses a method of producing a crystalline substrate based device comprising: providing a wafer (Figs.2-8 el.200) comprising a semiconductor microstructure (el.242) including a semiconductor substrate (col.3 lines 22-26); providing a spacer (el.236) at a wafer level, said spacer defining at least one cavity (el.264) extending entirely therethrough; adhesively sealing (col.5 lines 13-19) to said wafer at least one

Art Unit: 2813

transparent chip scale packaging layer (col.4 lines 65-67) and said spacer onto said semiconductor substrate over said microstructure and at least partially spaced therefrom, thereby to define at least one gap at said at least one cavity between said microstructure and said at least one chip scale packaging layer (Fig.3); forming a multiplicity of electrical contacts (el.306) along surfaces of said at least one packaging layer which define edges of individual chip scale packaged devices (Fig.8); and subsequently dicing said wafer into said individual chip scale packaged devices (el.292), wherein said spacer is formed as a piece separate from said substrate **[claims 20, 52, 53]**. Salatino also discloses forming a microstructure on a crystalline substrate (col.3 lines 27-30), and wherein said microstructure receives light via said at least one transparent chip scale packaging layer (col.5 lines 33-37) **[claims 39, 40, 64]**.

Based upon the rejection of claims 20, 39, and 52 above, Salatino also discloses wherein said adhesively sealing comprises using epoxy to seal said at least one transparent chip scale packaging layer and said spacer onto said substrate (col.5 lines 13-19) **[claims 22, 41, 54]**; wherein said crystalline substrate comprises silicon (col.3 lines 27-30) **[claims 23, 42, 55]**; wherein said at least one cavity comprises a plurality of cavities (col.4 line 65 – col.5 line 3) **[claims 26, 43, 59]**; wherein said microstructure comprises a micromechanical structure (col.5 lines 24-33) **[claims 27, 44, 60]**; wherein said microstructure comprises a microelectronic structure (col.4 lines 30-33) **[claims 28, 45, 61]**; wherein said microstructure comprises a surface acoustic wave device (col.5 lines 24-33) **[claims 34, 48, 63]**; and wherein said spacer is formed as a piece separate from said at least one chip scale packaging layer (Fig.3) **[claim 38]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 24, 33, 36, 47, 49-50, and 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salatino as applied to claims 20, 39, and 52 above, and further in view of Ichikawa et al. (5,996,199). Salatino does not disclose forming a microstructure on a quartz, lithium niobate, or lithium tantalate substrate. However, Salatino would look to one such as Ichikawa for proper light absorption because Ichikawa discloses wherein said crystalline substrate comprises lithium niobate (col.2 lines 51-54) [**claims 24, 50, 56**]; wherein said crystalline substrate comprises lithium tantalate (col.2 lines 51-54) [**claims 33, 47, 57**] and wherein said crystalline substrate comprises quartz (col.2 lines 51-54) [**claims 36, 49, 58**]. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the substrates of Ichikawa with the method of Salatino in order to absorb light of a particular frequency used in surface acoustic wave (SAW) devices (Ichikawa – col.15 lines 29-36).

Claims 29, 46, and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salatino as applied to claims 20, 39, and 52 above, and further in view of Malinovich et al. (6,168,965). Salatino does not disclose an optoelectronic

Art Unit: 2813

structure. However, Salatino would look to one such as Malinovich because Malinovich discloses wherein said microstructure comprises an optoelectronic structure (col.1 lines 5-8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the optoelectronic device of Malinovich with the method of Salatino, wherein an optoelectronic structure requires a transparent cover such as that disclosed by Salatino.

Claims 51 and 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salatino as applied to claim 39 above, and further in view of Chen (6,083,766).

Salatino does not disclose plating electrical contacts. However, Salatino would look to one such as Chen for a solderable surface because Chen discloses plating a multiplicity of electrical contacts along edge surfaces (col.4 lines 25-37). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the plating of Chen with the method of Salatino in order to obtain favorable soldering surfaces (Chen - col.4 lines 33-36) **[claims 51, 65]**.

Based upon the rejection of claim 65 above, Salatino also discloses wherein at least one gap is located over said crystalline substrate and under said at least one chip scale packaging layer (Fig.3) **[claim 66]**; and wherein said chip scale packaging layer is sealed over said microstructure by means of an adhesive (col.5 lines 13-19) **[claim 67]**.

Response to Arguments

Applicant's arguments with respect to claims 20, 22-24, 26-29, 33-34, 36, and 38 have been considered but are moot in view of the new ground(s) of rejection.

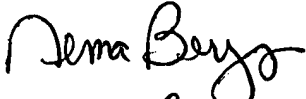
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB


Nema Berezny